'समानो मन्त्रः समितिः समानी'

UNIVERSITY OF NORTH BENGAL

B.Sc. Honours 3rd Semester Examination, 2021

CC7-PHYSICS

DIGITAL SYSTEMS AND APPLICATIONS

Time Allotted: 2 Hours | Full Marks: 40

The figures in the margin indicate full marks.
All symbols are of usual significance.

GROUP-A

1. Answer any ***five*** questions from the following: 1×5 = 5

   (a) Convert $(11000101)_2$ to hexadecimal.

   (b) Represent (–58) in 2's complement scheme.

   (c) Convert the Gray code 1101 to binary code and $(1010)_2$ to Gray code.

   (d) Justify: Compliment of XNOR is XOR.

   (e) Write "89" in 8 bit BCD.

   (f) Draw the state transition diagram for a MOD-10 counter.

   (g) Draw the output waveform of an astable multivibrator whose duty cycle is 75%.

   (h) Distinguish between Latches and Flip-Flops.

GROUP-B

Answer any *three* questions from the following 5×3 = 15

2. Design a full-adder circuit using only NAND gate. 5

3. Draw the logic symbol 4:1 multiplexer. Find its output equation and realise the equation using gates. 1+2+2

4. For a given logic equation $f(A, B, C) = AB + C$: $2\frac{1}{2}+2\frac{1}{2}$

   (i) Make a truth table

   (ii) Realise the circuit for the given equation using only NAND gates.

5. (a) How many flip-flops are required to build a binary counter that count from 0 to 1023? 2

(b) Determine the frequency at the output of the last flip-flop of this counter for an input clock frequency of 4 MHz. What is counter's MOD number? 2+1

6. Construct an even parity checker circuit and explain the working principle. 5

GROUP-C

Answer any *two* questions from the following 10×2 = 20

7. (a) Draw the circuit of 4:1 MUX and 1:4 DEMUX. How to make a 8:1 MUX using two 4:1 MUXs. 2+2+3

(b) What are the main difference between the demultiplexer and decoder? When a demultiplexer can be used as decoder? 2+1

8. What is the race around condition of a J-K flip-flop? Why does it occur? How it is resolved? Construct and explain the working principle of Master-Slave JK flip-flop with the help of timing diagram. What are the uses of Master-Slave JK flip-flop? 2+1+1 +5+1

9. (a) Draw the circuit diagram of a 4-bits serial input parallel output shift register when 4-bit output data will appear at the output simultaneously. Explain its operation with the help of timing diagram. 2+3

(b) What are the main disadvantages of asynchronous counter? Draw the circuit of a MOD-6 synchronous counter. Explain its counting pattern with state-transition diagram. 1+2+2

10.(a) Build up a unit RAM-cell using R-S flip-flop. Explain the working principle on storing 1-bit data into the cell and reading data from the cell. 5

(b) Design a monostable multivibrator using 555-timer IC with on-time of unstable state T is one sec. 2

(c) Explain with circuit diagram the operation of an astable multivibrator. 3

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